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EXAMINER
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STEVENS, THOMAS H

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/883,836

**Applicant(s)**

BAILEY ET AL.

**Examiner**

Thomas H. Stevens

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2001.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-36 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 17 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/6/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Claims 1-36 were examined.

#### ***Claim Interpretation***

2. Office personnel are to give claims their "**broadest reasonable interpretation**" in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See \*also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. Examiner interprets the word "consulting" as a bi-directional communication between simulators and "domain" is equivalent to the coordinated setup between the hardware and software simulation configuration (Klein reference: column 4, lines 15-20 with figure 1).

#### ***Specification***

3. The attempt to incorporate subject matter into this application by reference to titled "Synchronization of Multiple Simulation Domains in an EDA Simulation

Environment," is improper because of a missing application number and the phrase "incorporation by reference".

***Provisional Obviousness Double-Patenting Rejection***

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 9-13,15-29 and 35 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2-6,8-23 of copending Application No. 09/883,838 because the claims are identical.

For example, claim 9 of application 09/883,836 states the following:

- Claim 9. The method of claim1 wherein the plurality of simulation domains comprise at least one of a software execution domain a hardware simulation domain, and an abstract model simulation domain.

While claim 2 of application 09883,838 state the following:

- Claim 2. The method of claim 1 wherein the plurality of simulation domains comprises at least one of a software execution domain, a hardware simulation domain, and an abstract model simulation domain.

One of ordinary skill in the art at the time of invention would deduce that the preceding claims are identical. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

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art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The following statement is not clearly discussed within the specification: ***consulting*** system configuration information to determine which of the plurality of simulation domains corresponded to the particular system state.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The word “consulting” is unclear within the context of the claim.

### ***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-12,14-27,30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein (U.S. Patent 5,771,370 (1998)). Klein teaches a co-simulation of a hardware-software system is performed with a single coherent view of the memory of the hardware-software system (abstract).

Claim 1. A method comprising: identifying state information comprising (column 13, lines 45-50 with figure 18) a transfer from a first simulation model in a simulation environment, said transfer being directed to a second simulation model in a circuit design being simulation in the simulation environment (column 12, lines 21-31); receiving the state information from the first simulation model (section covers the relationship between software events: column 14, lines 43-53); and making the state information available to the second simulation model without simulating the transfer in the circuit design (section covers the relationship between software events: column 14, lines 43-53).

Claim 2. The method of claim 1(column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein simulating the transfer form the first simulation model to the second simulation model in the design (section covers the relationship between software events: column 14, lines 43-53) comprises transferring the state information through at least one additional simulation model in the simulation environment.

Claim 3. The method of claim 1 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein receiving the state information and making the state information available comprises: storing the state information in a coherent state memory space that is part of the simulation environment (column 11, lines 9-13) and corresponds to an element in the circuit design being simulated, said coherent state memory space being accessible to both the first simulation model and the second simulation model.

Claim 4. The method of claim 3 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 11, lines 9-13) wherein the coherent state memory space is accessible to a plurality of additional simulation models.

Claim 5. The method of claim 1 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein receiving the state information and making the state information available comprises at least one of: a virtual transfer path for use when a simulation model of a transfer path in the circuit design is not included in the simulation environment (column 14, lines 5-17); and a higher performance transfer path than the simulation model of the transfer path in the circuit design.



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Claim 6. The method of claim 5(column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 5-17) wherein the higher performance transfer path provides a lower level (specification defines logic simulations tend to operate at the lower levels of abstraction: column 5, lines 41-50) of resolution than the simulation model of the transfer path in the circuit design.

Claim 7. The method of claim 3 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 11, lines 9-13) wherein the simulation environment comprises a plurality of additional simulation models, each of the plurality of additional simulation models corresponding to one or more of a plurality of additional coherent state memory spaces (column 6, lines 53-56), the method further comprising: identifying additional state information comprising additional transfers among the plurality of additional simulation models in the simulation environment (columns 13-14, lines 65-67, 1-4, respectively); and storing the additional state information (column 11, lines 10-13) in appropriate ones of the plurality of additional coherent state memory spaces such that the additional state information is accessible to corresponding of the plurality of additional simulation models without simulating the additional transfer in the circuit design (column 14 ,lines 1-17).

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Claim 8. The method of claim 1(column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein the simulation environment comprises a plurality of simulation domains, the method comprising: selectively activating (column 2, lines 51-54) and deactivating particular simulation domains in the simulation environment (column 14, lines 18-26) such that a resolution and a performance for the circuit design being simulated is dynamically modified (abstract) as the state information is received and made available.

Claim 9. The method of claim1 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein the plurality of simulation domains comprise at least one of a software execution domain (column 18, lines 46-59), a hardware simulation domain, and an abstract model simulation domain.

Claim 10. The method of claim 9 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 18, lines 46-59) wherein the software execution domain comprises at least one of a native processor package, an instruction set simulator (ISS) (column 6, lines 20-25), and a programming language simulator (column 19, lines 16-41) to model software execution in one or more processors.

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Claim 11. The method of claim 9 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 18, lines 46-59) wherein the hardware simulation domain comprises at least one of a logic simulator (column 19, lines 16-41) and a programming language simulator.

Claim 12. The method of claim 11 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 18, lines 46-59) wherein the logic simulator comprises one of a hardware description language (HDL) (column 5, lines 45-48) based simulator, a gate-level simulator, a simulation accelerator, a system simulator (column 3, lines 44-45), a cycle simulator (column 5, line 280), and a programmable hardware emulator (column 2, line 5).

Claim 14. The method of claim 9 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 18, lines 46-59) wherein the hardware simulation domain comprises at least one simulation model of a circuit element in the circuit design (hardware designs: column 5, lines 41-45).

Claim 15. The method of claim 8 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12,

lines 21-31; column 14, lines 18-26;and abstract) further comprising: partitioning the circuit design (hardware designs: column 5, lines 41-45) into the plurality of simulation domains based on a partition criteria (column 7, lines 24-25).

Claim 16. The method of claim 15 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 7, lines 24-25) wherein the partition criteria comprises at least one of an abstraction level, (specification defines logic simulations tend to operate at the lower levels of abstraction: column 5, lines 41-50) a simulation type, and a function type (column 7, lines 40-41,48-50).

Claim 17. The method of claim 16 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 7, lines 24-25; column 7, lines 40-41,48-50) wherein partitioning the circuit design (column 7, lines 24-25) based on the abstraction level partition the circuit deign into at least one of a pin-level domain (column 2, lines 25-29), a bus-level domain (column 18, lines 28-30), and a transaction-level domain (column 1, line 64).

Claim 18. The method of claim 16 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 7, lines 24-25; column 7, lines

40-41,48-50) wherein partitioning the circuit design based on the simulation type partitions the circuit design into at least one of a software execution domain (column 18, lines 46-59), a logic simulator domain (column 19, lines 16-41), and a programming language simulator (column 19, lines 16-41) domain.

Claim 19. The method of claim 16 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 7, lines 24-25; column 7, lines 40-41,48-50) wherein partitioning the circuit design based on the function type comprises: identifying one or more function elements in the circuit design that have a particular level of independent operation from the remainder of the circuit design; and defining of a domain encompassing each identified functional element (inherent: a simple circuit design (i.e., resistors, capacitors, etc)).

Claim 20. The method of claim 8 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract) wherein each of the plurality of simulation domains provides a particular performance level and a particular resolution level, and wherein the particular simulation domains are selectively activated or deactivated during particular stages of simulation in combinations that either accelerate performance (design choice) of the simulation environment or increase resolution of the simulation environment (design choice).

Claim 21. The method of claim 8 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract) wherein selectively activating and deactivating the particular simulation domains comprises: identifying a system state of the circuit design; determining which of the plurality of simulation domains are to be active for the identifying system state (column 14, lines 44-53); and advancing simulation time only in each activated simulation domain (column 9, lines 30-47).

Claim 22. The method of claim 21 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract; column 14, lines 44-53; column 9, lines 30-47) wherein determining which of the plurality of simulation domains are to be active for the identified system state comprises at least one of a centralized control (column 5, lines 40-44), a transaction-based (column 1, line 64) control, and a distributed control.

Claim 23. The method of claim 22 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract; column 14, lines 44-53; column 9, lines 30-47; wherein the centralized control comprises: receiving the system state (column 14, lines 44-53) from one or more of the plurality of domains; consulting system configuration (column 4, lines 15-25 with figure 1) information to determine which of the

plurality of simulation domains correspond to the particular system state (Klein reference: column 4, lines 15-20 with figure 1); and instruction a centralized simulation clock (column 9, lines 30-40) to advance only for those domains corresponding to the particular system state.

Claim 24. The method of claim 22 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract; column 14, lines 44-53; column 9, lines 30-47) wherein the system state comprises system addresses in the circuit design.

Claim 25. The method of claim 22 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract; column 14, lines 44-53; column 9, lines 30-47) wherein the system state comprises a data transaction in the circuit design, said data transaction being configured with information identifying which of the plurality of simulation domains (Klein reference: column 4, lines 15-20 with figure 1) are to be active for the data transaction, and wherein the transaction-based control comprises: sending a message to a centralized simulation clock as part of the data transaction, said message to instruct the centralized simulation clock with respect to which of the plurality of simulation domains are to be active for the data transaction.

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Claim 26. The method of claim 22(column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 14, lines 44-53; column 9, lines 30-47) wherein a predetermined simulation domain is configured with activation information identifying at least one particular system state for which the predetermined simulation domain (Klein reference: column 4, lines 15-20 with figure 1) is to be active, wherein identifying the system state comprises receiving a broadcast of the system state at the predetermined simulation domain comprises (active cycle: column 3, lines 10-15) determining if the predetermined simulation domain is to be active for the identifying system state based on the activation information; and advancing an operation in the predetermined simulation domain according (column 10, lines 54-61).

Claim 27. The method of claim 26 (column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26;and abstract; column 14, lines 44-53; column 9, lines 30-47; column 10, lines 54-61) wherein the information further identifies an event for terminating operation of the predetermined simulation domain for the at least one particular system state (column 10, lines 44-47).

Claim 30. The method of claim 1(Klein: column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein both the first simulation model and the second



simulation model are within a same simulation domain (Klein reference: column 4, lines 15-20 with figure 1) in the simulation environment.

Claim 31. The method of claim 1, (Klein: column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein the first simulation model and the second simulation model are within different simulation domains (Klein reference: column 4, lines 15-20 with figure 1) in the simulation environment.

Claim 32. The method comprising: reading state information (column 13, lines 45-50 with figure 18) from a first simulation model in a simulation environment when a simulation domain of the first simulation model is deactivated; and writing the state information to a second simulation model in the simulation environment (column 12, lines 21-31) prior to activation of a simulation domain of the second simulation model, (section covers the relationship between software events: column 14, lines 43-53) said first simulation model and said second simulation model representing different version (design choice) of a same functionality in a circuit design being simulation.

Claim 33. The method of claim 32 (section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31) wherein the first simulation model and the second simulation model each have a particular level of performance and resolution, and wherein simulation of the circuit design switches from the first

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simulation model to the second simulation model is based on a change in a performance level (columns 13-14, lines 65-67, 1-18) and/or a resolution level desired at a difference stage of simulation.

Claim 34. The method of claim 32 (section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; columns 13-14, lines 65-67, 1-18) wherein the first simulation model and the second simulation model are among a plurality of simulation models representing a same functionality in the circuit design, each of the plurality of simulation models having a particular level of performance and resolution (not addressed: level of performance is undefined), and each of the plurality of simulation models being used at different stages of simulation depending on a desired performance (design choice) level and/or resolution level of the simulation.

Claim 35. A machine readable medium having stored thereon machine executable instructions (column 14, lines 43-53) that when executed implement a method comprising: identifying state information comprising a transfer from a first simulation model in a simulation environment, said transfer being directed to a second simulation model in a circuit design being simulation environment (columns 2-3, lines 56-67, 1-7); receiving the state information from the first simulation model (column 35-46); and making the state information available to the second simulation model without simulating the transfer in the circuit design (column 14, lines 50-53).

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Clam 36. A machine readable (column 14, lines 43-53) medium having stored thereon (column 11, lines 9-13) machine executable instructions that when executed implement a method comprising: reading state information from a first simulation model in a simulation environment when a simulation domain (Klein reference: column 4, lines 15-20 with figure 1) of the first simulation model is deactivated (columns 13-14, lines 65-67, 1-17, respectively); and writing the state information to a second simulation model in the simulation environment prior to activation of a simulation domain of the second simulation model (columns 13-14, lines 65-67, 1-17, respectively), said first simulation model and said second simulation model representing different versions (design choice) of a same functionality in a circuit design being simulated.

***Claim Rejections - 35 USC § 103***

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill

in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claim 13 is rejected under 35 U.S.C. 103 (a) as unpatentable by Aleksic et al., (U.S. Patent 5,995,736 (1999)), in view of Klein (U.S. Patent 5,771,370 (1998)). Aleksic et al., teaches integrated circuit modeling system using C/C++ and VHDL but doesn't model software and hardware. Klein teaches a co-simulation of a hardware-software system is performed with a single coherent view of the memory of the hardware-software system (abstract). At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Klein with Aleksic et al. to produce a software-modeling interface that precisely reflects the state of the device under design (Aleksic: column 3, lines 3-6).

Claim 13. The method of claim 11 (Klein: column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 18, lines 46-59) wherein the programming language simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, a simulator using a C-based language (Aleksic: column 4, line 41), a simulator using a C++ based language (Aleksic: column 4, line 41), and a JAVA (Aleksic: column 13, line 13) programming language simulator.

15. Claim 28 is rejected under 35 U.S.C. 103 (a) as unpatentable by Dave (U.S. Patent 6,178,542 (2001)), in view of Klein (U.S. Patent 5,771,370 (1998)). Dave teaches hardware-software co-synthesis algorithm is the process partitioning with the

use of a static scheduler based on deadline-based priority level; but doesn't have a platform to perform simulation. Klein teaches optimizing hardware (i.e., memory mapped (column 4, lines 45-46)) and software. At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Klein with Dave to negate concurrent co-synthesis of aperiodic and periodic task graphs with hard real-time constraints (Dave: column 3, lines 41-45).

Clam 28. The method of claim 21 (Klein: column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract; column 14, lines 44-53; column 9, lines 30-47) wherein determining which of the plurality of simulation domains (Klein reference: column 4, lines 15-20 with figure 1) are to be active for the identified system state depends on a plurality of control mechanisms, wherein each of the plurality of control mechanisms comprises a priority level, and wherein a higher priority control mechanism takes precedence over a lower priority control mechanism (Dave: column 12, lines 14-25).

16. Claim 29 is rejected under 35 U.S.C. 103 (a) as unpatentable by Eisenhofer et al., (U.S. Patent 6,339,836 (2002)), in view of Klein (U.S. Patent 5,771,370 (1998)). Eisenhofer et al., teaches a flexible automated design partitioning mechanism that facilitates simulation sessions employing two or more simulations with a hierarchical representation; but doesn't teach hardware-software co-simulation. Klein teaches

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optimizing hardware (i.e., memory mapped (column 4, lines 45-46)) and software. At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Klein with Eisenhofer et al. to provide an intelligence automated design partitioning to preserve name space mapping across partitions (Eisenhofer: column 2, lines 5-14).

Claim 29. The method of claim 8 (Klein: column 13, lines 45-50 with figure 18; section covers the relationship between software events: column 14, lines 43-53; column 12, lines 21-31; column 14, lines 18-26; and abstract) wherein the plurality of simulation domains comprises a hierarchical structure (Eisenhofer: column 7, lines 35-46) and wherein selectively activating and deactivating the particular simulation domains is based on levels of the hierarchical structure.

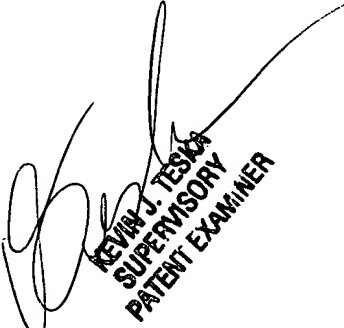
***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

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